ABSTRACT

Process for forming dual gate oxides for DRAM systems by using a "shadow effect" to control gate oxide thickness at AA corners adjacent a STI region, comprising:

I) a. forming AA by depositing over a semiconductor substrate, a patterned nitride layer exposing portions of the substrate to define an isolation region and a capacitor region within the isolation region;

b. etching exposed regions of substrate using patterned nitride layer to form isolation trench in isolation region and capacitor trench in capacitor region within isolation region;

c. oxidizing the substrate to form a thermal oxide layer in the isolation trench and the capacitor trench;

d. depositing oxide layer over thermal oxide layer to fill unfilled portions of isolation trench and capacitor trench;

e. removing patterned nitride mask;

f. planarizing substrate and forming a pad nitride strip;

II) forming sacrificial gate oxide layer on select locations of semiconductor substrate surface;

III) selectively etching sacrificial oxidation layer by using patterned resist as mask for channel implants;

IV) affecting channel implants for doping;

V) affecting masking so that nitrogen ions (N_2^+) to be implanted do not penetrate masked region; and

VI) causing nitrogen ion implantation by a "shadow effect" inducing means to provide lesser amounts of nitrogen ion dosage in inner part of active area adjacent the STI oxide than in remaining non-shadowed AA area, to provide increased thickness gate oxide at the AA corners.